Freescale Semiconductor
Application Note

Document Number: AN3349
Rev. 0, 10/2006

MPC5200B External Bus Options

by: Rick Nelson,
Regional Technology Specialist
Freescale Power Architecture™ and Netcomm

1 Introduction

The MPC5200B external buses can be defined as:

- An independent SDRAM bus capable of supporting SDR and DDR SDRAM devices.
- A LocalPlus bus capable of supporting three different bus protocols depending on how the MPC5200B address map (4 GByte) is defined:
  - Normal (multiplexed and/or non-multiplexed) memory cycles
  - PCI, V2.2, initiator, and target operations
  - ATA-4 Ultra-33 operation

This paper describes at a high level how data may be moved internally and externally through LocalPlus bus. The LocalPlus bus has a single set of address/data signals and separate normal, PCI, and ATA control lines. The LocalPlus bus interface is a multiplexed interface because it can be a normal, a PCI, or an ATA bus depending on which area of memory the current read/write transaction references.

Contents

1 Introduction 1
2 Chip Selects 2
3 Normal Mode 2
4 PCI Mode 3
5 ATA Mode 3

© Freescale Semiconductor, Inc., 2006. All rights reserved.

freescale™ semiconductor

2 Chip Selects

Identifying start/stop addresses for chip selects 0 – 7 and setting up base addresses in PCI base address registers 0 – 1, target base address translation registers 0 – 1, and the initiator window base/translation address register creates memory areas and controller assignments. Chip selects can support multiplexed or non-multiplexed modes and support different combinations of wait states, byte swapping, etc.

Section 3.3.2.2., "LocalPlus Bus," in the MPC5200B User's Manual explains the start/stop address registers. Two chip select start/stop address register pairs are associated with the LP_CS0 pin. One chip select start/stop register pair configures the LP_CS0 pin as the BOOT chip select in program space, and the other register pair configures the LP_CS0 pin to run normal memory access cycles in data space only. Only one of the LP_CS0 chip select start/stop address register pairs should be active at any given time. Only LP_CS0 can address program space and code execution. At BOOT time, the address space for LP_CS0 starts at 0x0000_0000 or 0xFFF0_0000 (depending on the reset configuration) and extends for 512 Kbytes by default. Chip select lines 1 – 7 can only select data space memory (Run-time program execution generally occurs from programs stored in the memory located on the SDRAM bus.). Chip select 4 and 5 can run normal memory cycles or are used during ATA cycles. Chip select 1 – 3 and 6 – 7 can only run normal memory cycles.

3 Normal Mode

Normal mode on the LocalPlus bus can consist of a multiplexed address/data external bus arrangement or non-multiplexed address/data external bus.

Multiplexed address mode has the ability to address larger ranges than the non-multiplexed mode because it incorporates two additional bank select lines. Through this mechanism, it supports addressing of 128 Mbytes total spread across four banks. Data size is limited to 32 bits max. The multiplexed address mode is the only mode that supports code execution. Additional logic is required to latch addresses and to decode bank selects. This mode is inherently slower than the non-multiplexed mode, but various address and data sizes are available on a chip select basis. Dynamic bus sizing is available in this mode.

Non-multiplexed mode consists of three sub-modes:

- Legacy mode
  - — Address/data lines limited to 32
  - — Supports small and medium group addresses
  - — Data sizes can be 8 or 16 bits
- Most graphics mode
  - — Address/data lines limited to 56
  - — Supports MOST group addresses
  - — Data sizes are 32 bits
- Large flash mode
  - — Address/data lines limited to 40 or 48 bits
  - — Supports large group addresses
  - — Data sizes can be 8 or 16 bits

Address ranges are also divided into three groups: small (8 and 16), medium/MOST (24 bit), and large (26 bit). Various data sizes are available within each address group. The non-multiplexed mode supports burst access.

The LocalPlus bus normal mode interface has a single half-duplex 512 Byte FIFO (32 words by 128 bits) to support DMA transfers between the LocalPlus Bus and memory using the DMA engine in the BestComm. Memory devices connected to LP_CS0 supports code execution and can function during BOOT operation. Refer to Table 9-2, Non-Muxed Options, in the MPC5200B User's Manual for specific BOOT options the reset configuration word can select.

4 PCI Mode

Section 10.6.2.1., "Address Translation," in the MPC5200B User's Manual explains the PCI base address registers (BAR) 0 – 1 and target base address translation registers (TBATR) 0-1. BAR0/TBATR0 is a 256 KByte range and BAR1/TBATR1 is a 1 GByte range. The initiator window base/translation address registers (IMWBAR) can be mapped to two 16 MByte or larger address spaces. The LocalPlus most graphics and large flash interfaces are not compatible with any PCI operation. When these interfaces are needed, the PCI internal controller must be disabled. However, even when the PCI internal controller is disabled, the PCI clock continues to be sourced by the MPC5200B. Two FIFOs (one for RX and one for TX) support the BestComm DMA engine that supports PCI interface, therefore, enabling full-duplex transfers.

5 ATA Mode

Ten registers that provide host configuration, status, and timing control ATA mode. The ATA interface has a half-duplex FIFO for DMA transfers controlled by the BestComm DMA engine. The BestComm DMA engine writes ATA commands into the ATA FIFO which initiates ATA read and write transactions. The BestComm DMA engine fills or empties the ATA FIFO data as needed. Any BestComm DMA transfers where the source and destination are resident on the LocalPlus bus require internal BestComm SRAM buffering.

What personality the LocalPlus Bus takes on for a given transaction depends on what particular defined MPC5200B memory space the transaction references. For example, for three different read and/or write transactions, the LocalPlus bus could be in normal bus mode for the first transaction, ATA bus mode for the second transaction, and PCI bus mode for the third transaction. What mode is active is entirely dependent on how the memory map, the start/stop, and PCI base registers are set up.

The MPC5200B can support SDRAM, local-normal, local-PCI, and local-ATA protocols in a given system simultaneously with some restrictions on local-normal modes. Realize the local, PCI, and ATA functions are multiplexed amongst themselves. Each peripheral has its own FIFO and associated FIFO controller, allowing all three modes (normal, PCI, and ATA) to function at the same time.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: AN3349
Rev. 0
10/2006

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals”, must be validated for each customer application by customer’s technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2006. All rights reserved.

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics as their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see http://www.freescale.com or contact your Freescale sales representative.

For information on Freescale’s Environmental Products program, go to http://www.freescale.com/epp.

freescale™
semiconductor